REMARKS

The Official Action mailed August 12, 2005, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Also, filed concurrently herewith is a *Request for Continued Examination*. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants appreciate Examiner Liang's time in conducting a personal interview on October 21, 2005. During the interview, for example with respect to claim 1, the Applicants stressed that the prior art references do not teach or suggest that a circuit produces a phase difference in a second signal with respect to a phase of a first signal and that both the first and second signals are input to each of a plurality of shift registers or latches. By providing a phase difference between the first and second signals, noise can be reduced in operation of a display device. Examiner Liang suggested that the advantage of noise reduction be incorporated into the claims. Therefore, the Applicants have amended the independent claims to clearly recite the above-referenced features and the advantage of noise reduction.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on May 21, 1999, and April 14, 2004.

Claims 1, 3-10, 12-17, 19-23, 25-35 and 37-45 were pending in the present application prior to the above amendment. Dependent claims 9, 15, 22, 34 and 45 have been canceled without prejudice or disclaimer, independent claims 1, 8, 14, 21, 27 and 33 have been amended to better recite the features of the present invention, and the title and dependent claims 7, 13, 20, 26, 32 and 38 have been amended to correct a minor matter of form. Accordingly, claims 1, 3-8, 10, 12-14, 16, 17, 19-21, 23, 25-33, 35 and 37-44 are now pending in the present application, of which claims 1, 8, 14, 21, 27 and 33 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

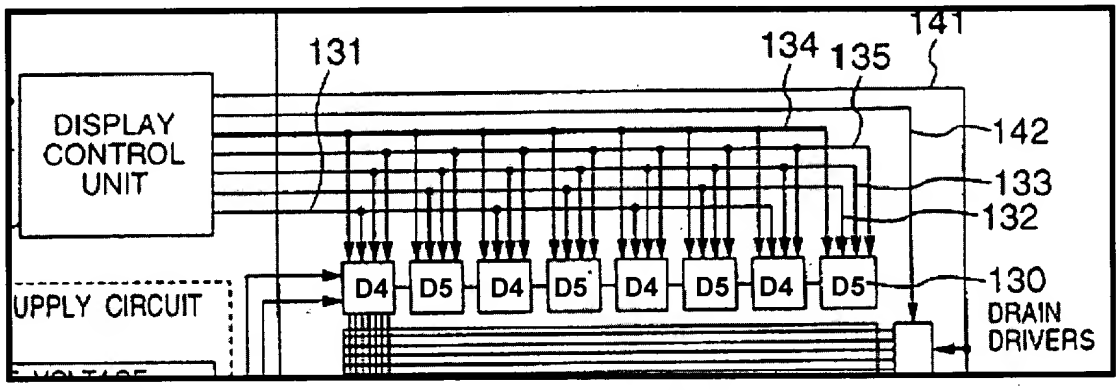
Paragraph 3 of the Official Action rejects claims 1, 3-6, 8-10, 12, 14-17, 19, 21-23, 25, 27-31, 33-35, 37 and 39-45 as obvious based on the combination of U.S. Patent No. 6,229,513 to Nakano et al. and U.S. Patent No. 5,734,378 to Okada et al. The Applicants respectfully submit that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. The independent claims have been amended to recite that a circuit produces a phase difference in a second signal with respect to a phase of a first signal and that both the first and second signals are input to each of a plurality of shift registers or latches and that noise is reduced in a display device. Nakano and Okada do not teach or suggest that signals D4 and D5 should be

input to each of a plurality of shift registers or latches or that noise is reduced in a display device.

Nakano discloses the following: "The clock signal D4 is transmitted to a group A of drain drivers 130 (odd-numbered drain drivers 130 in FIG. 1) through a signal line 131. The clock signal D5 in turn is transmitted to a group B of drain drivers 130 (even-numbered drain drivers 130 in FIG. 1) through a signal line 132" (column 6, lines 32-37).



As clearly shown in Figure 1 of Nakano (annotated above), signal D4 is input to alternating drain drivers 130 and signal D5 is input to other alternating drain drivers 130.

Nakano states that the clock signal D4 is transmitted to a group A of drain drivers (odd-numbered drain drivers 130 in Figure 1) through a signal line 131. The clock signal D5 in turn is transmitted to a group B of drain drivers 130 (even-numbered drain drivers 130 in Figure 1) through a signal line 132 (column 6, lines 31-36). While both signals enter the drain drivers 130 when considered as a whole, the first signal D4 and second signal D5 are input to only the odd or even drain drivers 130, respectively. Therefore, both signals are not input to every shift register 153 in a control circuit 152 of drain drivers 130.

Figure 7 of Nakano shows further detail of each drain driver 130 as follows:

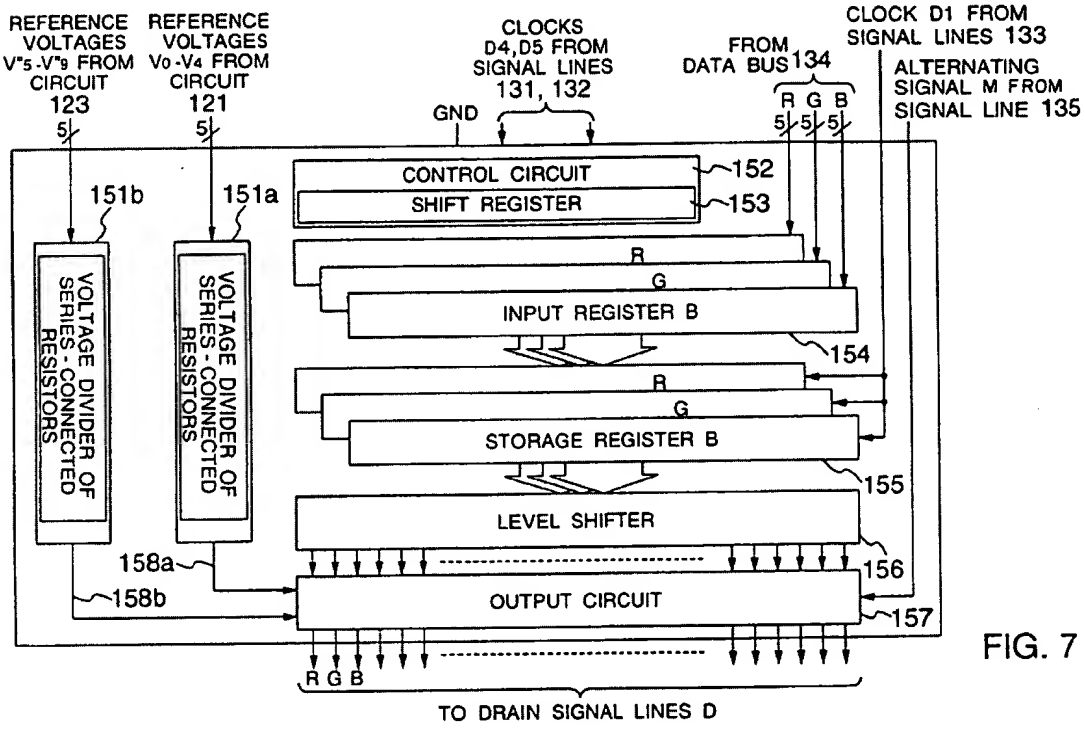


FIG. 7

Nakano teaches that a "shift register 153 in a control circuit 152 of the drain driver 130 generates a data fetch signal for an input register 154 based on a clock signal D4 or D5 for latching display data inputted from the display control unit 110" (column 9, lines 61-65, emphasis added). From Figure 1 and Figure 7 of Nakano, it is clear that only one of signal D4 or D5 is provided to each of drain drivers 130. It is further clear from Figure 7 that each drain driver 130 includes shift register 153 (and shift register 153 does not extend across multiple drain drivers 130). Since signals D4 and D5 are not input to the same drain driver 130, Nakano does not teach or suggest that signals D4 and D5 are input to each of a plurality of shift registers or latches.

Still further, Okada does not cure the deficiencies in Nakano. The Official Action asserts that "Okada teaches a control circuit of a display device having a delay circuit (40 in Fig. 2) for producing a phase difference (Φ) in a second signal (CK') with respect to a phase of a first signal (CK)" (page 3, Paper No. 20050809). The Applicants

respectfully disagree and traverse the above-referenced assertion in the Official Action. Okada is not directed to a phase difference between two clock signals applied to the same circuit. Rather, Okada merely appears to teach delaying a single clock signal (CK). The delayed clock signal CK' is used so "that data can be latched in the drivers 25 and 27" (column 8, lines 3-4; Figure 3). As such, it is not clear how or why one of ordinary skill in the art would have applied the teachings of Okada directed to a single clock signal CK (converted to CK') to first and second clock signals D4 and D5 of Nakano, much less teach or suggest that signals D4 and D5 should be input to each of a plurality of shift registers or latches.

Therefore, Nakano and Okada, either alone or in combination, do not teach or suggest a circuit that produces a phase difference in a second signal with respect to a phase of a first signal and both the first and second signals are input to each of a plurality of shift registers or latches.

Since Nakano and Okada do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained.

Furthermore, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Nakano and Okada or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be modified in the manner asserted in the Official Action, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

The test for obviousness is not whether the references "could have been" combined or modified as asserted in the Official Action, but rather whether the

references should have been. As noted in MPEP § 2143.01, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original). Thus, it is respectfully submitted that the standard set forth in the Official Action is improper to support a finding of *prima facie* obviousness.

The Official Action asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control circuit of Nakano to have a delay circuit as taught by Okada in order to produce a second clock signal having a different phase from the first clock signal" (page 3, Paper No. 20050809). The Applicants respectfully disagree and traverse the above-referenced assertions in the Official Action.

As noted in detail above, Okada merely teaches delaying a clock signal to ensure data can be latched as shown in Figure 3 and generally relates to multiplexing. Okada discloses that an upper bit and a lower bit of image data are transmitted via the same transmission line by using a time series data generator including a delay circuit so as to reduce the number of data lines included in the transmission line of a delay circuit. Nakano discloses that two groups of drain drivers are provided in order to lower the frequency of clock signals as described above. It is not clear why one of ordinary skill in the art who was concerned with producing a delayed clock signal CK' would not have simply practiced Okada alone. That is, it is not sufficient to merely point out the advantages of two references individually and assert that it would have been obvious to combine the two references so that you can have both advantages in one device. Rather, in order to form a *prima facie* case of obviousness, the Official Action must show that the references should have been combined.

Further, the signals produced from Okada's delay circuit are not used in the same way as in the present invention. As noted above, Okada teaches delaying a single clock signal (CK), thus producing a delayed clock signal CK' and is not directed

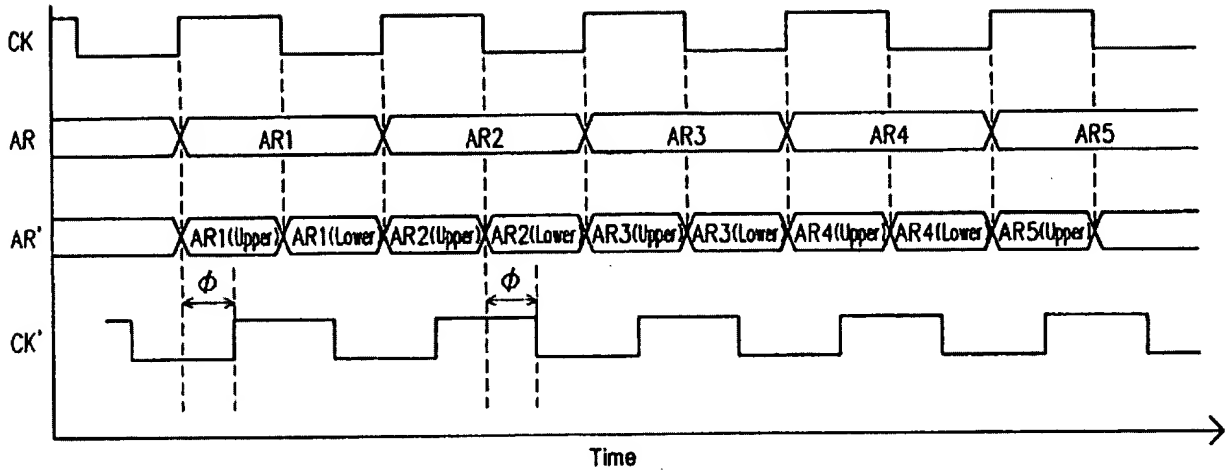
to two separate clock signals and clearly does not disclose or suggest that both CK and CK' are input to each of a plurality of shift registers or latches.

Nakano attempts to solve the "difficulties in sending a high frequency clock signal (D3) from a display control unit to drain drivers when using a high resolution liquid crystal display panel which is required with an increase in screen size of a liquid crystal display panel; and difficulties in taking countermeasures for preventing unnecessary radiation, even if a high frequency clock signal (D3) could be sent" (column 2, lines 52-58). Nakano has employed multiple clock signals in order to achieve a lowering in the frequency to this end.

Okada attempts to provide a display driving device which can be mass produced in which the increase in number of data lines and the increase in number of input terminals of a driver as the number of bits is increased can be suppressed and provides a data transfer method used in the device. Okada teaches that two sets of image data are transmitted via one data line in order to achieve suppression of the increase of data lines.

The Applicants respectfully submit that it is unclear as to why one skilled in the art at the time of the present invention and who was interested in the reduction of electromagnetic interference (EMI) would combine Nakano and Okada, which produce opposite results.

Fig. 3



As shown in Figure 3 (reproduced above), Okada's invention transmits two image data signals via one data line, which reduces the number of data signals, but, in doing so, also converts a low frequency signal into a high frequency signal. It is this high frequency signal that produces EMI. Therefore, one skilled in the art and interested in reducing EMI would not consider modifying Nakano with Okada. The delay circuit in Okada is used to merely align the timing of the clock signal and a high frequency image data signal. Therefore, it would not have been obvious to one skilled in the art to modify Nakano with Okada since it would have been counterproductive to do so. Even if one were to try to combine Nakano and Okada, the present invention could not be obtained.

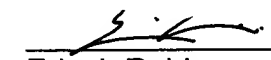
In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 3 of the Official Action rejects dependent claims 7, 13, 20, 26, 32 and 38 as obvious based on the combination of Nakano, Okada and U.S. Patent No. 5,801,678 to Shimada. Shimada does not cure the deficiencies in Nakano and Okada. The Official Action relies on Shimada to allegedly teach the features of the dependent claims. However, Nakano, Okada and Shimada, either alone or in combination, do not teach or suggest a circuit that produces a phase difference in a second signal with respect to a phase of a first signal and both the first and second signals are input to each of a plurality of shift registers or latches; or that noise is reduced in a display device. Since Nakano, Okada and Shimada do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Also, Shimada does not teach or suggest that it would have been obvious to combine Nakano and Okada. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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